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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,624	11/20/2003	Ju-Yong Lee	2522-036	3486

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EXAMINER	
ESTRADA, MICHELLE	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,624	LEE ET AL.	
	Examiner	Art Unit	
	Michelle Estrada	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *1-16,37 and 38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,18,20-26,28-33,39 and 40* is/are rejected.

7)☒ Claim(s) *19,27,34-36 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 17, 25 and 39 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17, 18, 20-26, 28-33, 39 and 40 rejected under 35 U.S.C. 102(b) as being anticipated by Liaw et al. (5,874,359).

Re claim 17, Liaw et al. disclose forming a first insulating film (11) on a semiconductor substrate (10); forming a wiring on the first insulating film (16') wherein the wiring includes conductive film patterns and a second insulating film patterns (20) formed on the conductive film patterns; forming a third insulating film (50) on the wiring and the first insulating film using a silicon oxide based material; forming contact patterns (52) on the wiring wherein the contact patterns define contact hole regions (7); forming contact spacers (54) on sidewalls of the contact patterns; and etching the third insulating film (50) and the first insulating film (11) using the contact patterns and the contact spacers as masks to form the contact holes (9) and to simultaneously form third insulating film patterns on sidewalls of the wiring (See fig. 11).

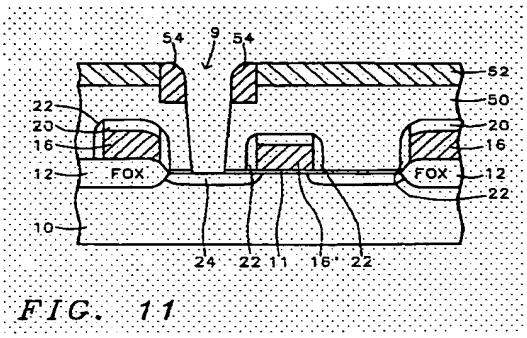

FIG. 11

Re claim 18, Liaw et al. disclose further comprising planarizing a predetermined portion of the third insulating film positioned on the wiring before forming the contact patterns (Col. 6, lines 1-3).

Re claim 20, Liaw et al. disclose wherein the contact pattern is formed to have a sufficient thickness to protect the third insulating film during the etching process for forming the contact holes.

Re claim 21, Liaw et al. disclose wherein the contact patterns are wider than the wiring.

Re claim 22, Liaw et al. disclose wherein the contact spacer has a sufficient thickness to overlap a portion of the first insulating film.

Re claim 23, Liaw et al. disclose wherein the contact pattern and the contact spacer comprise materials having etching selectivities relative to the third insulating film.

Re claim 24, Liaw et al. disclose wherein the contact pattern comprises polysilicon (Col. 6, lines 7-8) and the contact spacer comprises polysilicon (Col. 6, lines 46-48).

Re claim 25, Liaw et al. disclose forming a first insulating film (11) on a semiconductor substrate (10) having capacitor contact regions; forming bit lines (16') on the first insulating film between the capacitor contact regions wherein the bit lines include first conductive film patterns and second insulating film patterns (20) formed on the first conductive film pattern (16');

forming a third insulating film (50) on the bit lines and on the first insulating film wherein the third insulating film includes a silicon oxide based material; forming contact patterns (52) on the bit lines wherein the contact patterns define storage node contact hole regions (7); forming contact spacers (54) on sidewalls of the contact patterns; and etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the storage node contact holes and to simultaneously form third insulating film patterns on sidewalls of the bit lines (See fig. 11).

Re claim 26, Liaw et al. disclose further comprising planarizing a predetermined portion of the third insulating film positioned on the bit lines before forming the contact patterns (Col. 6, lines 1-3).

Re claim 28, Liaw et al. disclose wherein the contact pattern has a sufficient thickness to protect the third insulating film during an etching process for forming the storage node contact holes.

Re claim 29, Liaw et al. disclose wherein the contact patterns are wider than the bit lines.

Re claim 30, Liaw et al. disclose wherein the contact spacer has a sufficient thickness to overlap a portion of the capacitor contact region.

Re claim 31, Liaw et al. disclose wherein the contact pattern and the contact spacer comprise materials having etching selectivities relative to the third insulating film.

Re claim 32, Liaw et al. disclose wherein the contact pattern comprises polysilicon (Col. 6, lines 7-8) and the contact spacer comprises polysilicon (Col. 6, lines 46-48).

Re claim 33, Liaw et al. disclose after forming the storage node contact holes, further comprising: forming a second conductive film (56) on the contact patterns, the contact spacers

and the storage node contact holes wherein the second conductive film fills up the storage node contact holes; and planarizing the second conductive film by an etch back process to form storage node contact plugs in the storage node contact holes wherein the storage node contact plugs are connected to the capacitor contact regions (Col. 7, lines 58-66).

Re claim 39, Liaw et al. disclose forming a first insulating film (11) on a semiconductor substrate (10); forming a patterned conductive layer (16') on the first insulating film; forming a third insulating film (50) overlying the patterned conductive layer and the first insulating film; forming contact patterns (52) on the patterned conductive layer, the contact patterns defining contact hole regions (7) there between; forming contact spacers (54) on sidewalls of the contact patterns; and etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the contact holes (9) and to concurrently form third insulating film patterns on sidewalls of the patterned conductive layer.

Re claim 40, Liaw et al. disclose further comprising forming a second insulating layer pattern (20) overlying the patterned conductive layer.

Allowable Subject Matter

Claim 19, 27, 34-36 and 41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Estrada whose telephone number is 571-272-1858. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michelle Estrada
Patent Examiner
Art Unit 2823

ME
August 23, 2005